Dr. Prerana VijayKumar Rathod

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Summary: I am presently working as Head of Department and have worked in various positions. I have 32+ years of industry and teaching experience. Have closely worked with industry as a consultant. I am a merit list ranker with excellent academic performance and maintained distinction throughout. Have completed Masters in Technology (VLSI Technology) with first rank and PhD in SKVM's NMIMS, Mumbai. Have published several papers in journals of international repute and actively involved in holistic development of students.

Head of Department, Government Polytechnic Nashik [22nd June 2018 till Date]
Head of Department, Government Residential Womens Polytechnic Latur[27th October 2016 to 21st June 2018]

- Academic and administrative management of the department.
- NBA accreditation of Department from 1st July 2019 till 30th June 2025.
- Development of Curriculum-21 and Curriculum-23
- Chief coordinator for DTE sponsored FDP titled "Design and Development of Microstrip Patch Antennas and Wearable Antennas for Wireless Communication"
- Efforts to improve institute-Industry-Interaction
- Handled various portfolios at state, regional and institute level.

Shri Gulabrao Deokar College of Engineering (Formerly known as Shri Sureshdada Jain College of Engineering, Jalgaon [Jan' 2001 to 26th October 2016]

As a Professor, Academic Dean and Head of Department (Electronics & Telecommunication)

- Coordinating the planning, development, and assessment of academic program.
- Promoting and serving as a model for teaching and research.
- Chairman of Research and development, Quality circle and Students potential development committee.
- Continuous development and planning of basic infrastructure of the department.
- Responsible for development & setting of all laboratories.
- Convener and Coordinator of workshops and seminars for students and faculty at institute, university and National level.
- Able to motivate students to work and experiment beyond syllabus.
- Have taught various courses for undergraduate level like, Elements of Electronics Engg, Electronic Devices and Circuits-I & II, Digital Electronics, Analog Electronics, Linear Integrated Circuits, Electronics Measurements & Instrumentation, Microprocessor and Microprocessor Interfacing Circuits, Electronic Circuit Design, Very Large Scale Integration Design
- Was granted lien leave for 2 years to work as faculty for M. Tech(VLSI Technology) in North Maharashtra University Jalgaon.(From 1st July 2011 to 30 th June 2013)
- Have taught various courses for post graduate level like Digital Integrated Circuit, Analog VLSI, RF Integrated Circuits etc.

NATELCO, Nasik and STMF Consultancy services[Feb' 1992 to May' 2000]

As a consultant [Jan' 93 to Dec' 00]

- Developed changed Number Announcement System, L-Com and Subscriber 1+1 system and other related products.

As a Research & Development Engineer [Feb 92 to Dec' 92]

- Developed EPBAX, types of telephone instruments, test jigs for telecom products & microprocessor based systems

Sejda TV, Nasik [Aug '1991 to Feb 1992]

As a Trainee Engineer

- Quality assured production by testing television receivers.

ACADEMIC QUALIFICATIONS:

- PhD (Engineering), July 2014, from SKVM's NMIMS , Mumbai under guidance of Dr. B .K. Mishra (Principal TCET, Mumbai),
  Topic: "Modeling of MOSFET under Illumination for Optoelectronic Applications" where model validation was done by industry level tool SILVACO TCAD.
  Twelve papers were published linking them to the theory and methodology adopted.
- M.Tech (VLSI Technology), 2007 – from North Maharashtra University, Jalgaon (78.25%) with Distinction and **1st rank**.

  Topic: "Optimization Techniques for DCT Implementation" The core was developed using Xilinx ISE and optimized to meet timing requirement for Divinet Access Technologies Ltd, Pune.
- B.E (Electronics & Telecommunication), 1991 – Pune University , Maharashtra Institute of Technology, Pune- Distinction (66%) with **4th rank in institute**.
- HSC, 1987 – Maharashtra Board, RYK College, Nasik – Distinction (90%) **21st rank in merit list** of Pune Board.
- SSC, 1985 – Maharashtra Board – RJEMS Nasik –Distinction (87.85%) 2nd **rank in school.**

APPROVAL DETAILS:

- Approval as lecturer in North Maharashtra University, from 1st Jan 2004. (Ref No. NMU/18/J-58/5792/2004)
- Approval as Assosciate Professor in North Maharashtra University from 27th June 2009. (Ref No. NMU/18/310/2010).

PROFESSIONAL ACHIEVEMENTS:

- More than 20 research papers published in International Journals, International and National Conferences.
- Proficiency on tools like Xilinx ISE, Simon, QUCS, MATLAB, PSPICE, HPSICE, Tanner, GSS and SILVACO TCAD.
- Guided more than 30 students for M. Tech and M.E.
- Participation in various training and Faculty Development Programs

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AREAS OF INTEREST FOR RESEARCH:

- Semiconductor Device Modeling.
- VSLI Design: Front end and Back-end.
- Image Processing.

PROFESSIONAL AFFILIATIONS:

- Lifetime membership of Indian Society for Technical Education.
- Associate member of Institute of Engineers

RESEARCH PUBLICATIONS:

Journal Papers:

[1] G.Phade, **Prerana Jain** and B.K. Mishra ,'Modeling of Optical Effects of MOSFET with EKV3 in MATLAB" *in InJoREST - International Journal of Research in Engineering Science & Technology,*Vol 1 No.1, pp 55-61, June 2010.

[2] **Prerana Jain**, B.K. Mishra and G. Phade," Power Gain Analysis of Optically Illuminated MOSFET", *International Journal of Computer Applications'* Vol 51 No 16, August-2012, pp.50-54. (00975-8887)
Publisher and Place of Publication: Published By FCS® (Foundation of Computer Science) USA.

[3] **Prerana Jain** and, B.K. Mishra," C-V Investigation in Optically Illuminated MOSFET ", *International Journal of Engineering Research and Applications*, ,Vol. 2, No 6, pp.1282-1288, November-December 2012, , (2248-9622)
Publisher and Place of Publication: Published By IJERA ,India.

[4] **Prerana Jain** and B.K. Mishra," An Investigation of DC Characteristics in Multifinger Optically Illuminated MOSFET", *International Journal of Computer Applications'* Vol 61-No 2, January -2013. , pp.12-17. (00975-8887).
Publisher and Place of Publication:
Published By FCS® (Foundation of Computer Science) USA.

[5] **Prerana Jain** and B.K. Mishra," Evaluation of Optically Illuminated MOSFET characteristics by TCAD Simulation" , *International Journal of VLSI Design and Communication Systems*', (VLSICS)Vol 4 No 2, April 2013, pp11-25.
Publisher and Place of Publication: Academy And Industry Research Collabration Centre (AIRCC),India.

[6] **Prerana Jain** and B.K. Mishra," High frequency noise performance in OG-MOSFET", *Journal Of Electron Devices,*Vol No.18,August 2013,pp 1531-1536,(1682-3427)
Publisher and Place of Publication: Perpignan University,France

[7] A.J.Patil, **Prerana Jain** and Ashwini Pachpande, "Automatic Brain Tumor Detection Using K-Means and RFLICM" in International Journal of Innovative Research in Science, Engineering and Technology (IJIRSET),Volume 3-Issue 12,DECEMBER 2014, pp 13896-13903 ISSN ONLINE(2278-8875) PRINT (2320-3765)
Publisher and Place of Publication: Ess & Ess Research Publications, Chennai-600070, Tamilnadu, India

[8] Khairnar Vinayak Prakash, Abhijeet Kumar and **Prerana Jain, "**Circumventing Short Channel Effects in FETs: Review**"** International Journal of Computer Applications ,(IJCA) Volume 117 - Number 17**,** May 2015 (pp-24 -30), (2321-7545)
Publisher and Place of Publication: Published By FCS® (Foundation of Computer Science) USA.

[9] **Prerana Jain,** A.J.Patil and Mayuri Thakre," Floating point Arithmetic, International Journal of Scientific Research and Education(IJSRE***)***, Volume 3, Issue 07, July 2015, pp 3929-3936 (2321-7545)

[10] **Prerana Jain,** A.J.Patil, Prasad Kulkarni, " Development of Economical Monitoring system for vehicle security, International Journal of Innovations and Advancements in computer Science ,Volume 4, Issue -7,pp 64-67(2347-8616)
Publisher and Place of Publication: Academic Science,New Dehli

[11] Khairnar Vinayak Prakash, Abhijeet Kumar and **Prerana Jain,"** Simulation And Characterization Of Silicon Nanowire FET Using SILVACO TCAD", IJRIT International Journal Of Research In Information Technology, Volume 3, Issue 8, August 2015, Pg. 91-98 (2001-5569)

[12] **Prerana Jain,** A.J.Patil and Mayuri Thakre, " Synthesis and Simulation of Floating point Multipliers", International Journal of Advance Foundation and Research in Computer (IJAFRC), Volume 2, Issue 11, November - 2015. (2348 – 4853)

International Conferences:

[1] **Prerana Jain**, B.K. Mishra and S.C. Patil, " Capacitance Modeling of Optically Gated MOSFET' *in proceedings of ACM, ICWET 10 (International Conference and Workshop on Emerging Trends in Technology),* Pages 887-891 , ISBN: 978-1-60558-812- doi: 10.1145/1741906.1742109.

[2] B.K. Mishra, **Prerana Jain**, G.Phade and S.C. Patil," Optically Controlled Transconductance Amplifier", *in proceedings of ACM, ICWET 11(International Conference and Workshop on Emerging Trends in Technology),* ICWET 2011", Pages 1139-11423,ISBN:978-1-4503-0449-8 ,doi: 10.1145/1980022.1980266 .

[3] G.Phade, B.K. Mishra and **P. Jain,"** Small Signal Modeling of Illuminated MOSFET for RF application" *in proceedings of ACM, ICWET 11(International Conference and Workshop*

on Emerging Trends in Technology), ICWET 2011", Pages 1114-1119ISBN:978-1-4503-0449-8 ,doi: 10.1145/1980022.1980262 .

[4] **Prerana Jain**, Mishra B.K. and G, Phade, "AC performance of optically controlled MOSFET" in *proceedings of IEEE Students conference Electrical, Electronics and Computer Science* (SCEECS), 2012, ISBN: 978-1-4673-1516-6, doi :10.1109/SCEECS.2012.6184825,March-2012.

[5] **Prerana Jain**, Mishra, B.K. and G. Phade, "S parameters of optically illuminated MOSFET," in *proceedings of International Conference on Advancements in Engineering & Management* (ICAEM-2012) pp 9-12,February-2012.

Place and institute of Conference:

[6] Gaytri M Phade, B K Mishra and **Prerana Jain, "**Modeling of Optically Tailored Noise Parameters of MOSFET", *in proceedings on International Conference in Computational Intelligence (ICCIA2012)* iccia(8):-, March 2012.

[7] Mukesh Mahajan, Prasant Ingale, P.N.Jain, "FPGA Implementation of ARM Processor", *in proceedings of International Conference on Recent Technologies,* at Institute of knowledge college of Engineering, Pune, Feb 9-11, 2012.

[8] Tanay Dahale, Prashant Ingale , P.N.Jain, "Simulation and Analysis of Silicon Nanaowire Transistor" in proceedings of *International Conference on Recent Technologies*, at Institute of Knowledge college of Engineering, Pune Feb 9-11, 2012.

[9] Prerana Jain and A.J. Patil, "Implementation of two dimensional DCT core by pipelining" *in proceeding of International Conference on "Science, Engineering and Spirituality"* (ICSES-10) , on April 1st & 2nd, 2010, at SES College of Engineering, Navalnagar, Dhule (MS).

[10] Archana Shewale and Prerana Jain, " Face recognition using neutral network" *in proceeding of "International Conference on Science, Engineering and Spirituality*", (ICSES-10), on April 1st & 2nd, 2010, at SES College of Engineering, Navalnagar, Dhule (MS).

[11] **Prerana Jain,** A.J. Patil and Gayatri M Phade," FPGA Implementation of a Two Dimensional DCT Core" in *proceeding of International Conference on on Emerging Techniques in Computing, Electronics, Embedded System & VLSI Design*, on March 21-22, 2008, at Ahmednagar.

[12] Gayatri M Phade, R.S. Jahagirdar and Prerana Jain, "Intelligent Reflectometer for flexible pavement" at International Conference on Advances in Computing at Anuradha Engineering, February 25-26,2008, College, Chikli.

National Conferences:

[1]B.K. Mishra **,Prerana Jain**, and G.Phade, "I-V characterization of Optically Gated MOSFET" *in proceedings of National conference on Emerging Trends(NCET -10)* ,pp 183-187, March-2010.

[2]B.K. Mishra, G.Phade, and **Prerana Jain**, "InGaAs MISFET capacitances under illumination" *in proceedings National conference on Emerging Trends –(NCET-10),*pp158-160, March-2010.

[3]**Prerana Jain**, B.K. Mishra, G. Phade ,"RF performance of Optically Gated MOSFET" *in proceedings National conference on Emerging Trends –(NCET-10),*pp 57-61, March-2011.

[4] **Prerana Jain and** Archana Shewale," ERP and Web technology" *in proceedings of National conference on Computing, Communication, Electronica"* on 8-9 February, at KCE's College of Engineering and Information Technology, Jalgaon.

Book Chapters Published:

Partial Reconfiguration with AES Algorithm, Lambert Publishing House

PROFESSIONAL ACTIVITIES:

- Organizer & Convener of various workshops (PLC, Aurduino, PSPICE, Automation etc), conferences (ACME) etc. at Institute, State and University level.
- Invited to deliver expert lectures by Savitribai Phule Pune University, North Maharashtra University, Jalgaon and Sandip Foundation Nasik for post graduate students.
- Invited as session chair and judge for conferences and technical events.
- Worked as Subject expert, Paper–setter and Examiner for Amravati, Goa University at under-graduate and post graduate level.
- Attended Workshops on PSPICE, MATLAB, La-Tex, Labview and Semiconductor Device Modeling.
- Successfully completed workshop on 'High Impact Teaching skills' conducted by WIPRO and Dale Carnegie Associates.
- Trained on Virtuso Custom IC Design Flow at Cadence Training Centre, Bangalore.
- Coordinator for Avishkar-2013 where 10 groups were shortlisted for university and two groups represented university at State level.
- Actively involved in syllabus revision at university level.

SELECTIONS/HONOURS/ACHIEVEMENTS:

- First rank in M Tech (VLSI Technology) in North Maharashtra University.
- 21st ranking in merit list of HSC in Pune Board.
- Appreciation for volunteering faithfully and diligently as Jury for Engineering Talent Search Hosted by Laghu Udyog Bharti.
- Certificate by The International Association of Lions Club, Deolali Nashik-Road Club on International Womens Day for Contribution in Engineering.
- Final year graduation project sponsored by Motorola, USA.

EXTRA CURRICULAR ACTIVITIES:

- Counseling and guidance to parents of mentally retarded children
  (Course taken by Institute for achievement of Human Potential, USA)